S01P1860
仮図面

FIG.1

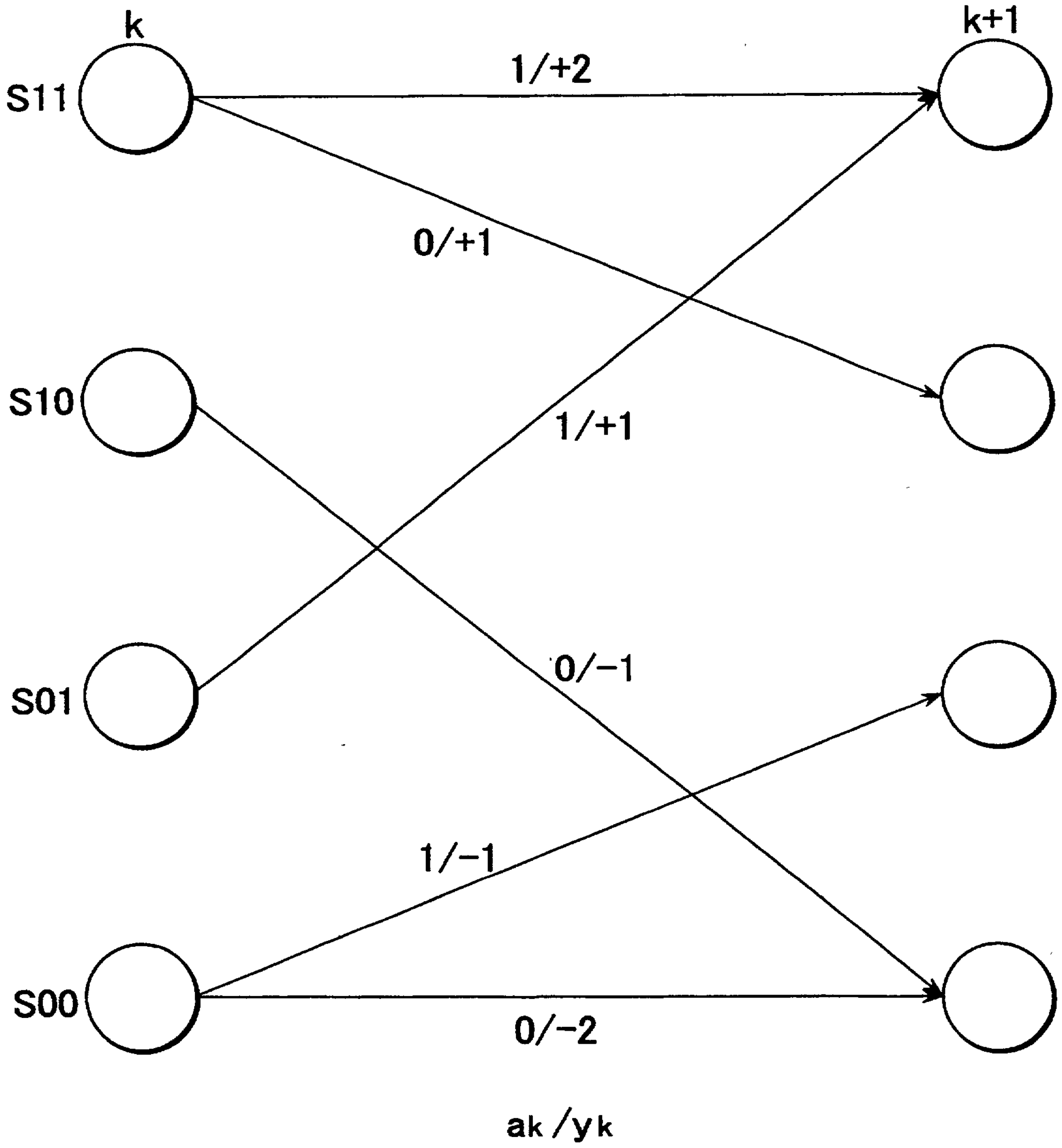

k
k+1
S11
S10
S01
S00
1/+2
0/+1
1/+1
0/−1
1/−1
0/−2
ak /yk

FIG.2

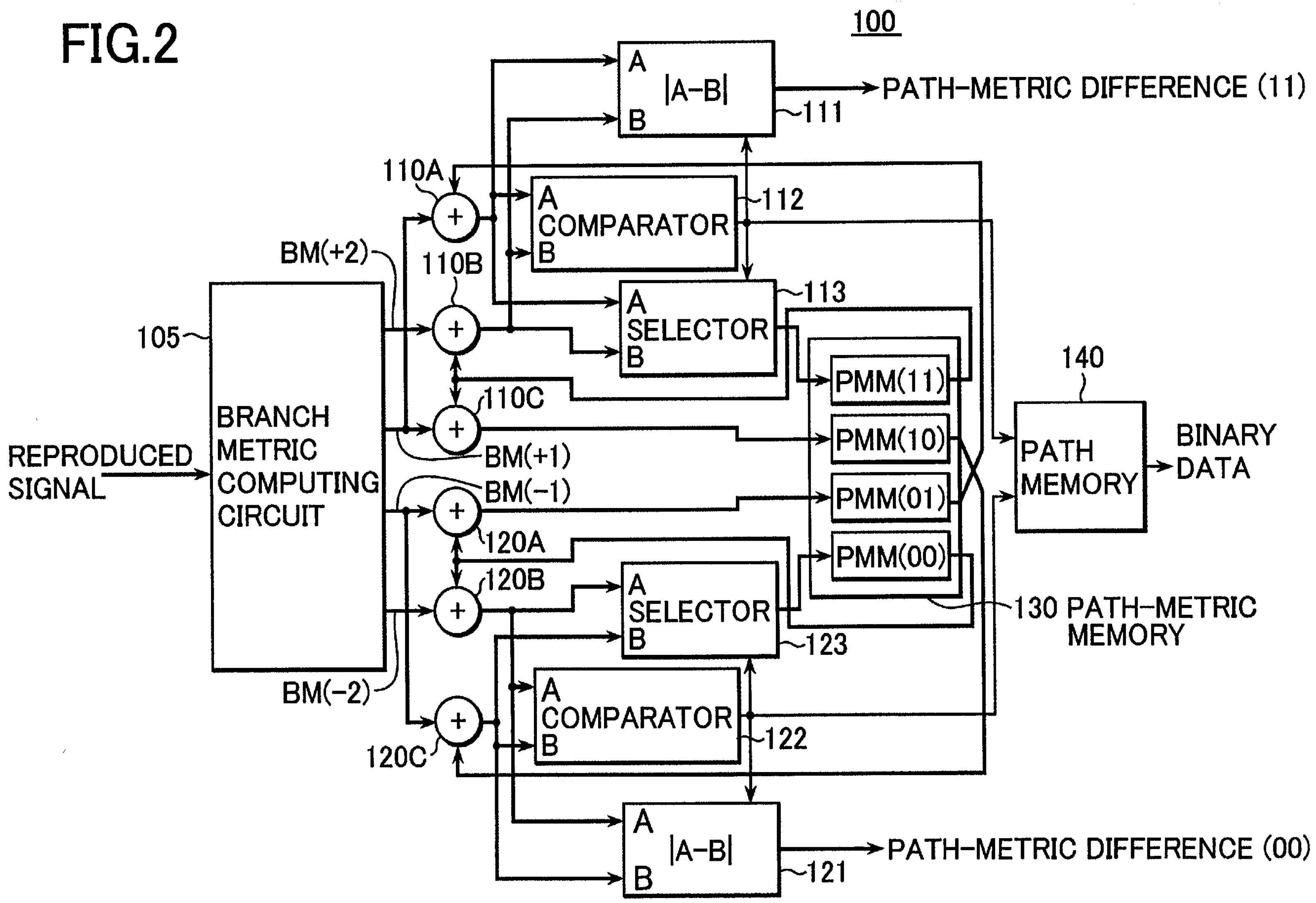

100
REPRODUCED SIGNAL
105
BRANCH METRIC COMPUTING CIRCUIT
BM(+2)
BM(+1)
BM(-1)
BM(-2)
110A
110B
110C
120A
120B
120C
+
A
|A-B|
B
111
PATH-METRIC DIFFERENCE (11)
A
COMPARATOR
B
112
A
SELECTOR
B
113
PMM(11)
PMM(10)
PMM(01)
PMM(00)
130 PATH-METRIC MEMORY
A
SELECTOR
B
123
A
COMPARATOR
B
122
A
|A-B|
B
121
PATH-METRIC DIFFERENCE (00)
140
PATH MEMORY
BINARY DATA

FIG.3

BINARY DATA ARRAY	SAM
00	PATH-METRIC DIFFERENCE(00)
01	VOID
10	VOID
11	PATH-METRIC DIFFERENCE(11)

FIG.4

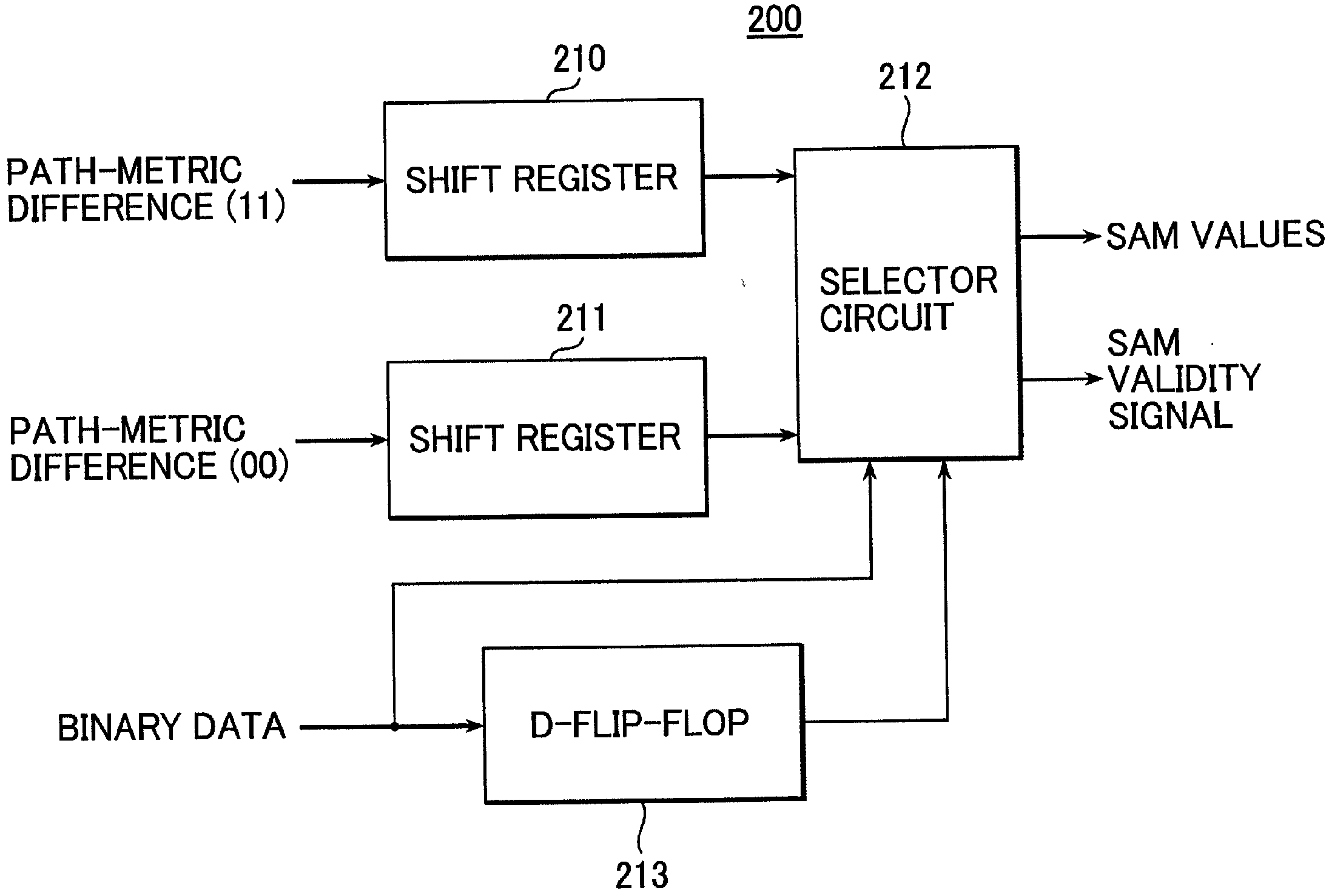

200
210
211
212
213
PATH-METRIC DIFFERENCE (11)
PATH-METRIC DIFFERENCE (00)
BINARY DATA
SHIFT REGISTER
SHIFT REGISTER
D-FLIP-FLOP
SELECTOR CIRCUIT
SAM VALUES
SAM VALIDITY SIGNAL

FIG.5

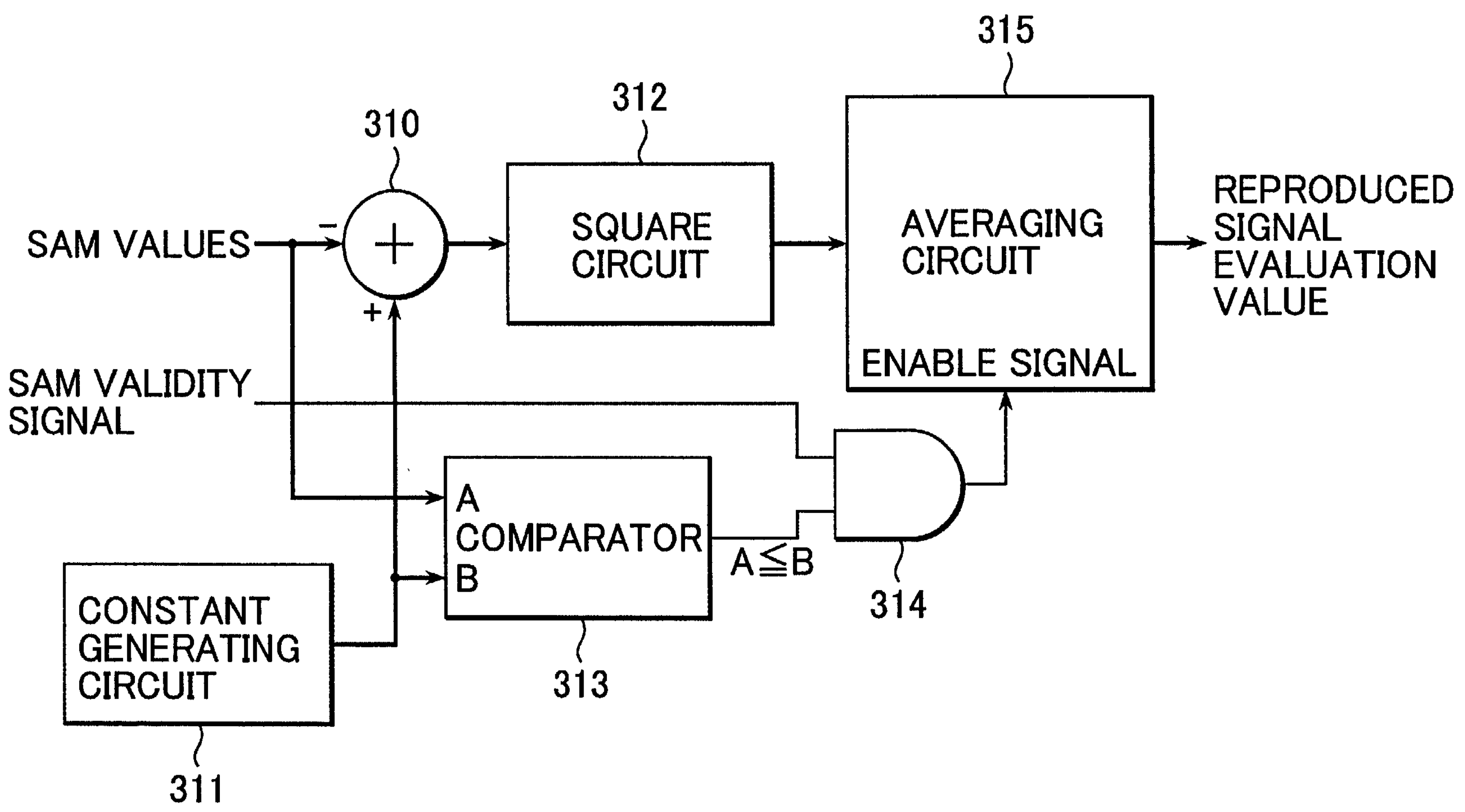

310
312
315
SAM VALUES
−
+
SQUARE CIRCUIT
AVERAGING CIRCUIT
ENABLE SIGNAL
REPRODUCED SIGNAL EVALUATION VALUE
SAM VALIDITY SIGNAL
A
COMPARATOR
B
A≦B
314
313
CONSTANT GENERATING CIRCUIT
311

FIG.6

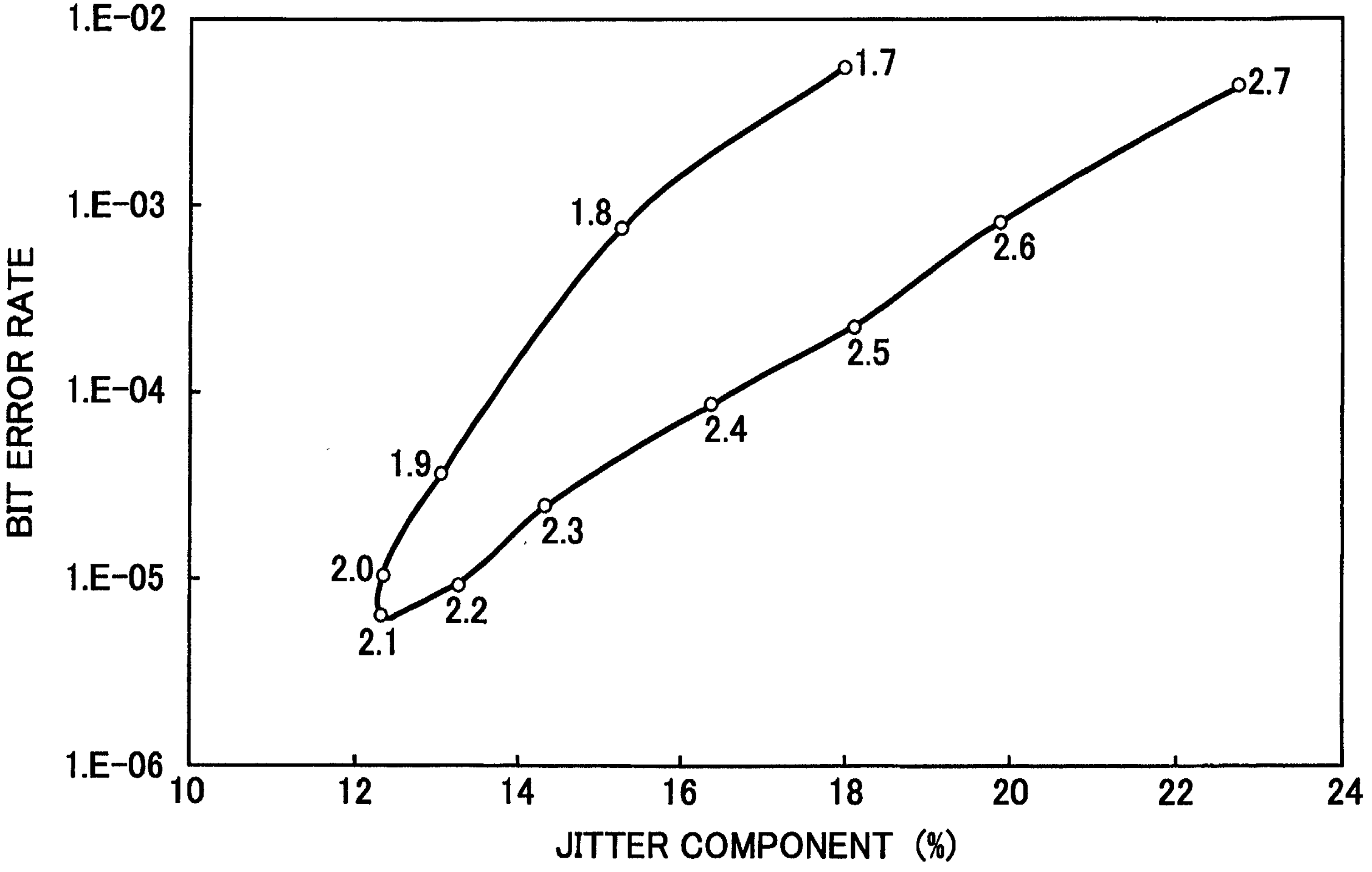

1.E-02
1.E-03
1.E-04
1.E-05
1.E-06
BIT ERROR RATE
10
12
14
16
18
20
22
24
JITTER COMPONENT (%)
1.7
1.8
1.9
2.0
2.1
2.2
2.3
2.4
2.5
2.6
2.7

FIG.7

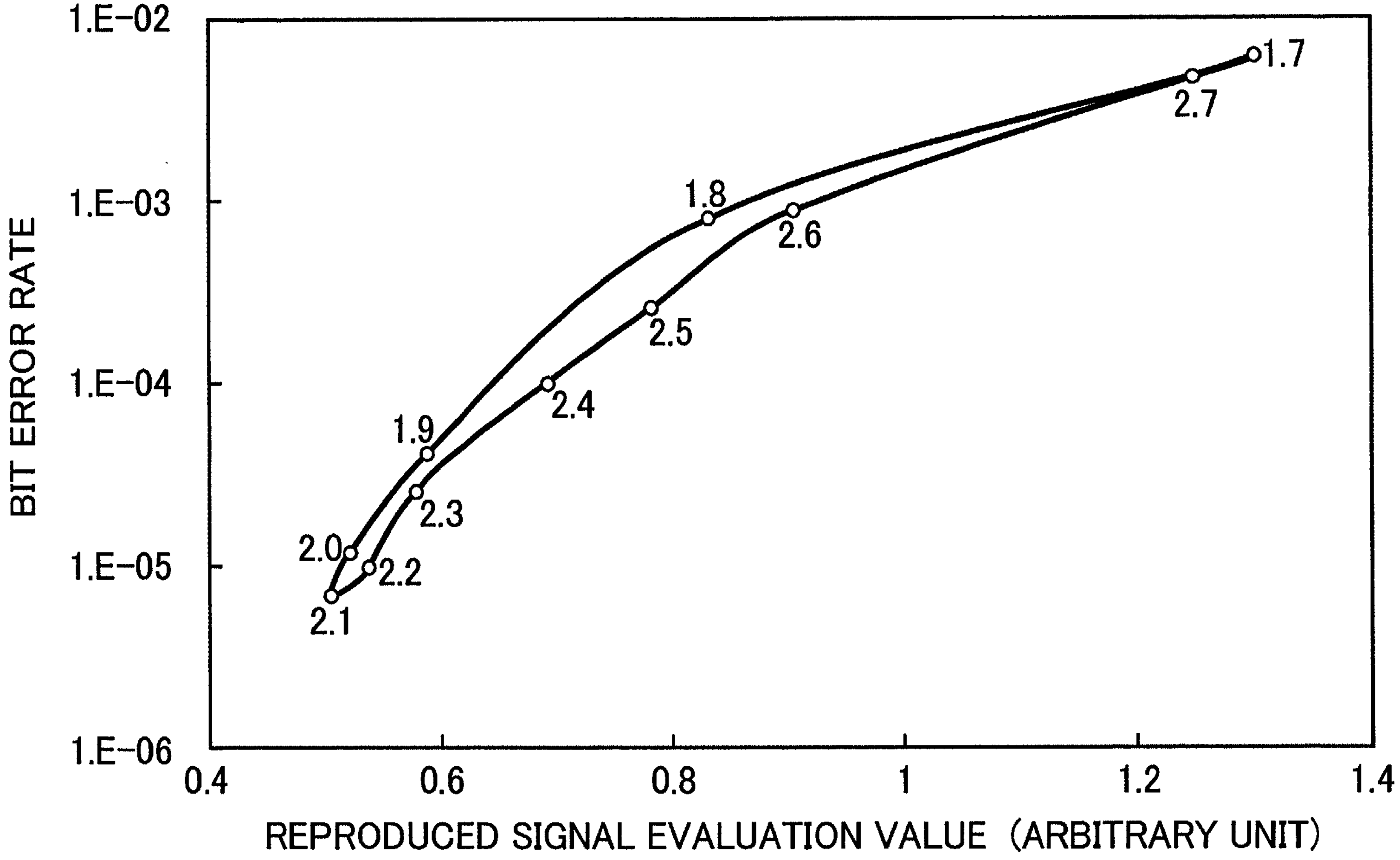

1.E-02
1.E-03
1.E-04
1.E-05
1.E-06
BIT ERROR RATE
0.4
0.6
0.8
1
1.2
1.4
REPRODUCED SIGNAL EVALUATION VALUE (ARBITRARY UNIT)
1.7
1.8
1.9
2.0
2.1
2.2
2.3
2.4
2.5
2.6
2.7

FIG.8

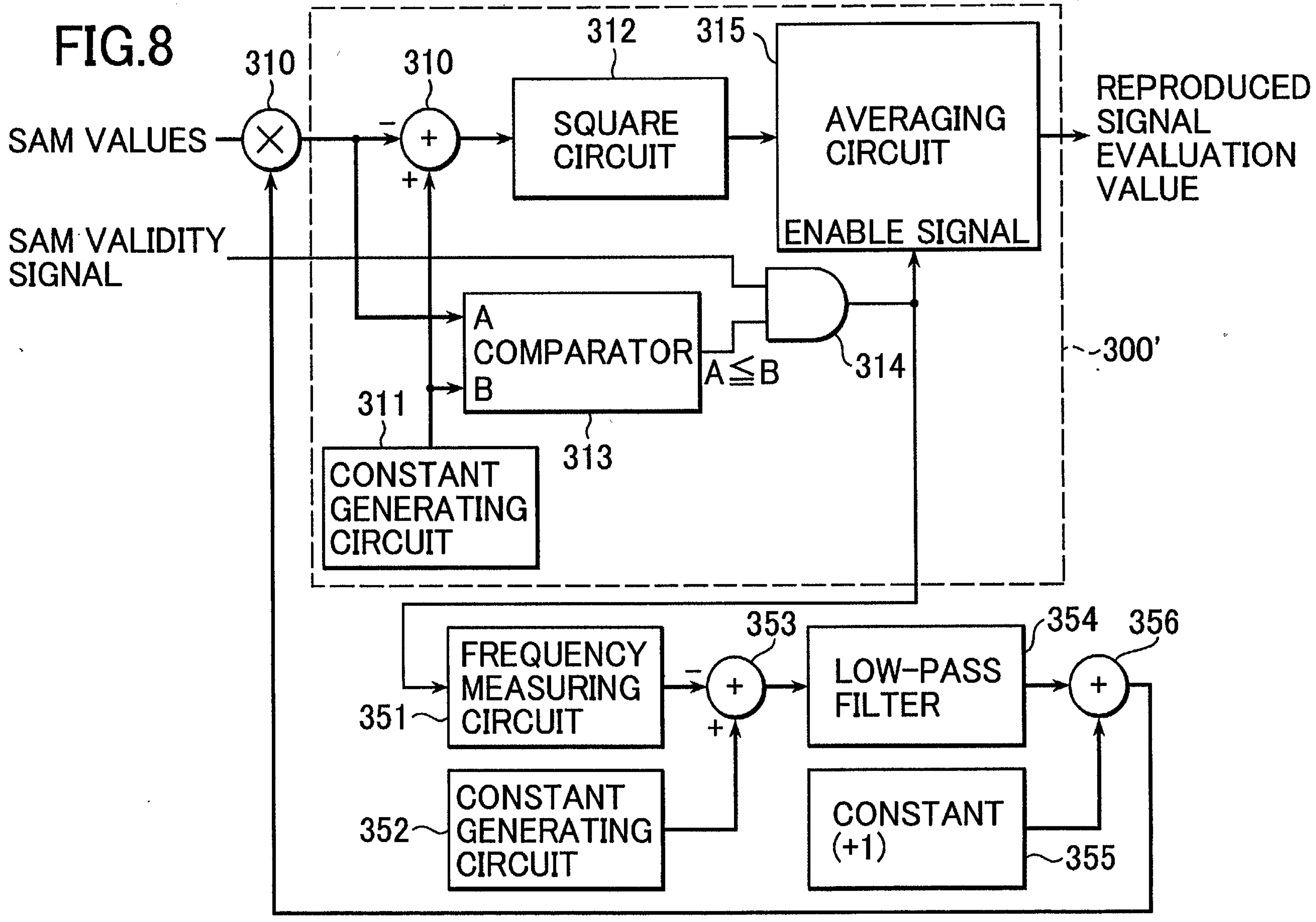

SAM VALUES
SAM VALIDITY SIGNAL
310
310
−
+
312
SQUARE CIRCUIT
315
AVERAGING CIRCUIT
ENABLE SIGNAL
REPRODUCED SIGNAL EVALUATION VALUE
A
COMPARATOR
B
A≦B
314
300'
311
CONSTANT GENERATING CIRCUIT
313
353
354
356
FREQUENCY MEASURING CIRCUIT
351
−
+
LOW-PASS FILTER
352
CONSTANT GENERATING CIRCUIT
CONSTANT (+1)
355

FIG.9

SAM VALUES WITHOUT CORRECTION

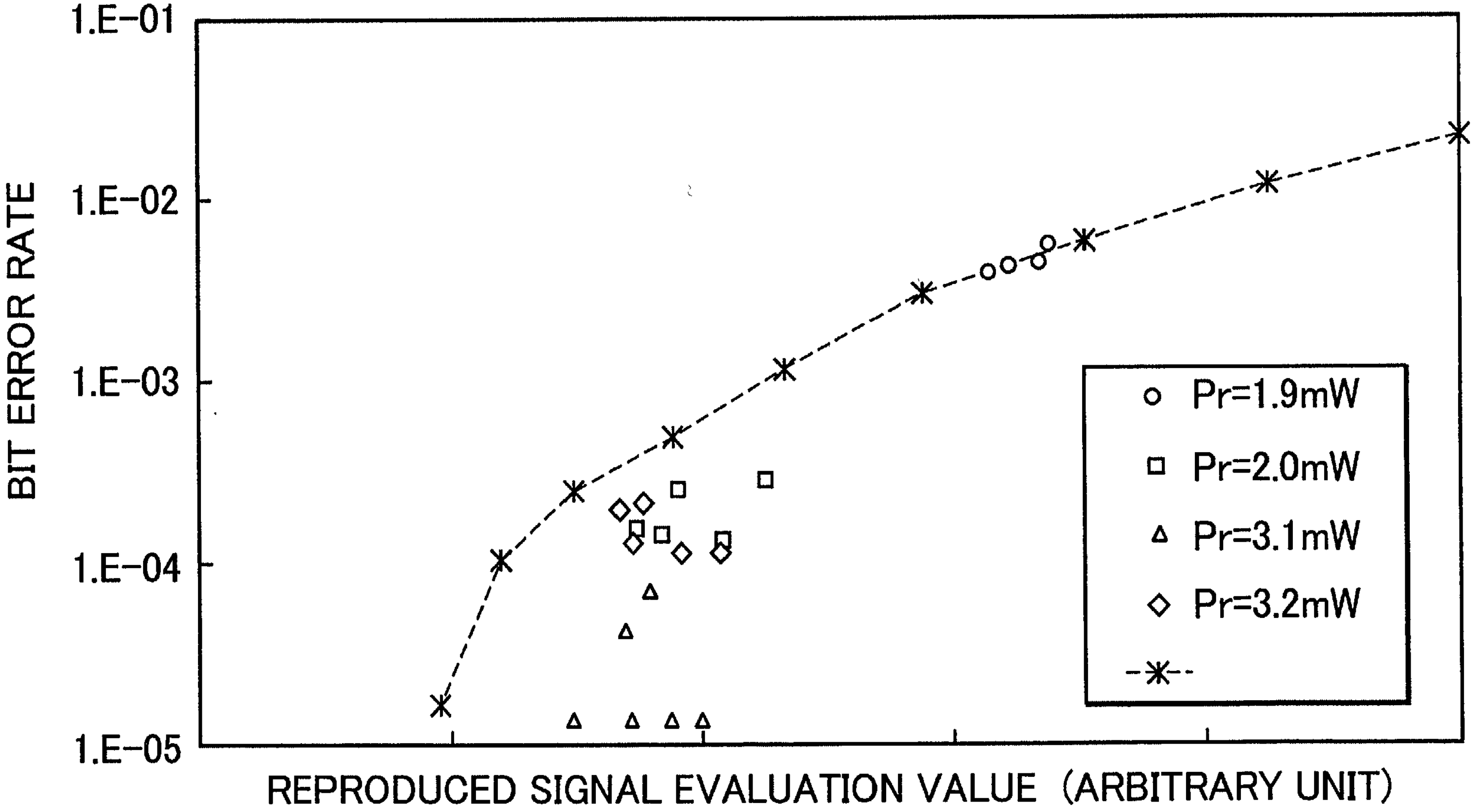


FIG.10

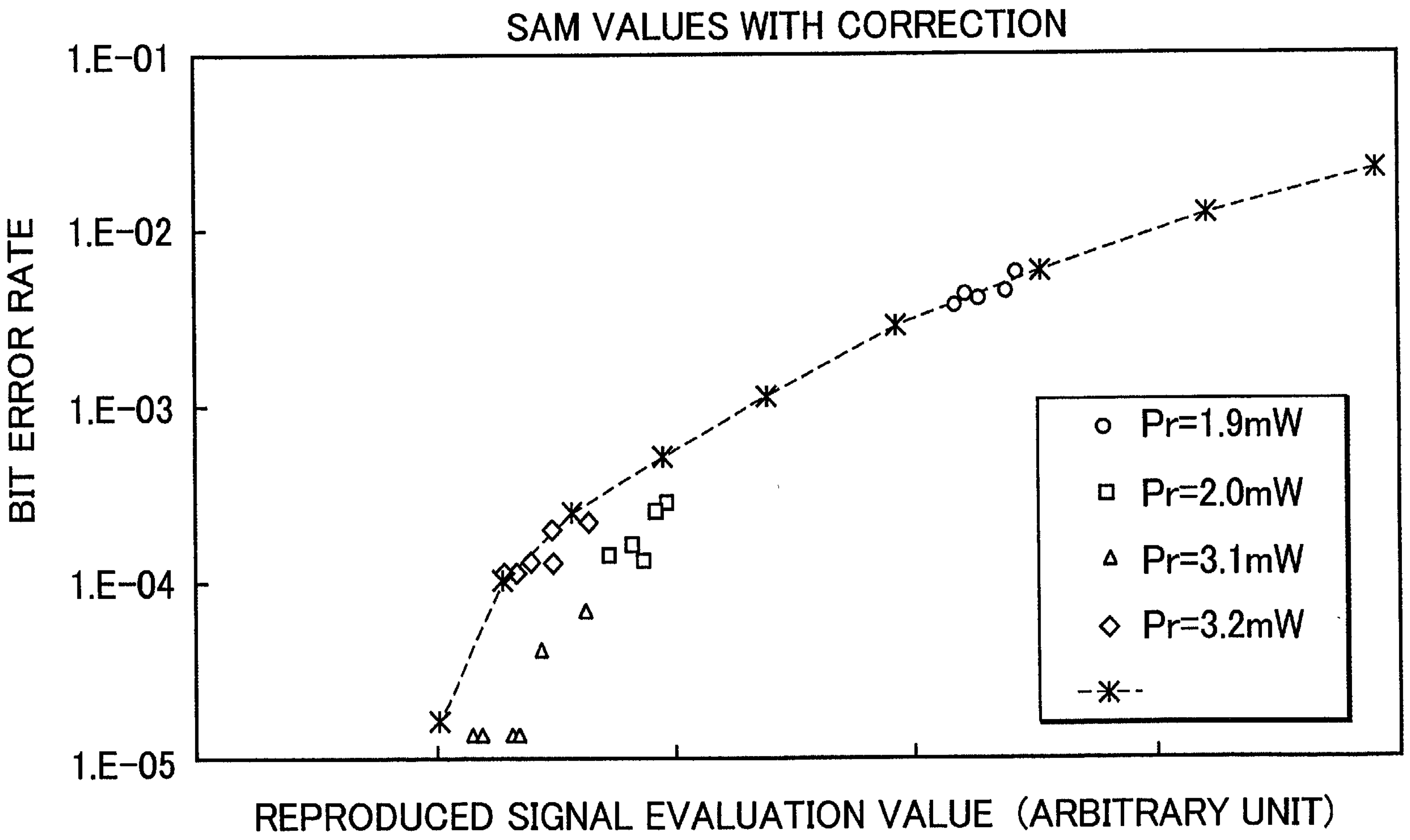
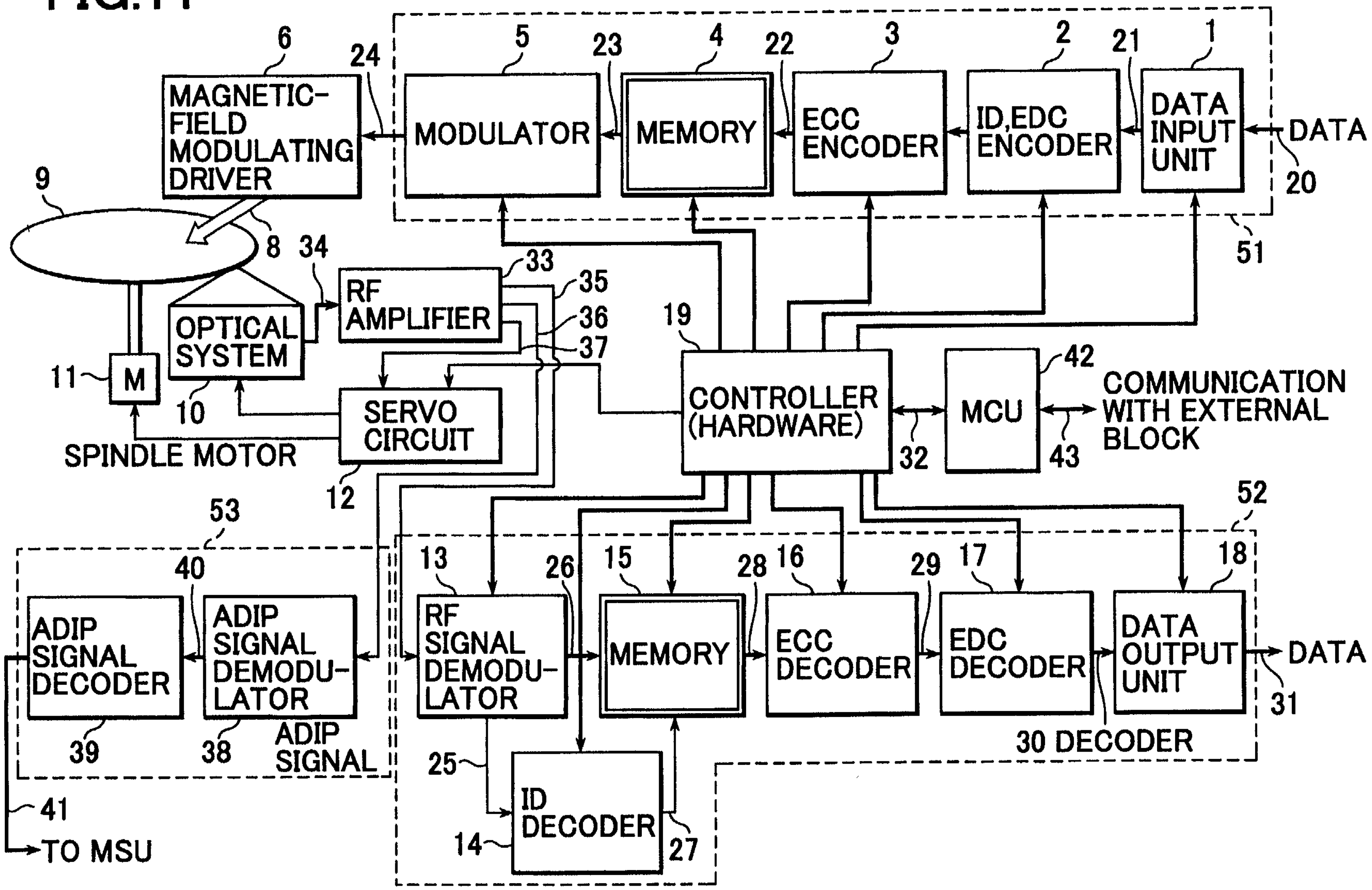

SAM VALUES WITH CORRECTION
BIT ERROR RATE
1.E-01
1.E-02
1.E-03
1.E-04
1.E-05
REPRODUCED SIGNAL EVALUATION VALUE (ARBITRARY UNIT)
○ Pr=1.9mW
□ Pr=2.0mW
△ Pr=3.1mW
◇ Pr=3.2mW
-✱-

FIG.11



MAGNETIC-FIELD MODULATING DRIVER
MODULATOR
MEMORY
ECC ENCODER
ID,EDC ENCODER
DATA INPUT UNIT
DATA
OPTICAL SYSTEM
RF AMPLIFIER
M
SERVO CIRCUIT
SPINDLE MOTOR
CONTROLLER (HARDWARE)
MCU
COMMUNICATION WITH EXTERNAL BLOCK
ADIP SIGNAL DECODER
ADIP SIGNAL DEMODULATOR
ADIP SIGNAL
TO MSU
RF SIGNAL DEMODULATOR
MEMORY
ECC DECODER
EDC DECODER
DATA OUTPUT UNIT
DATA
30 DECODER
ID DECODER

FIG.12

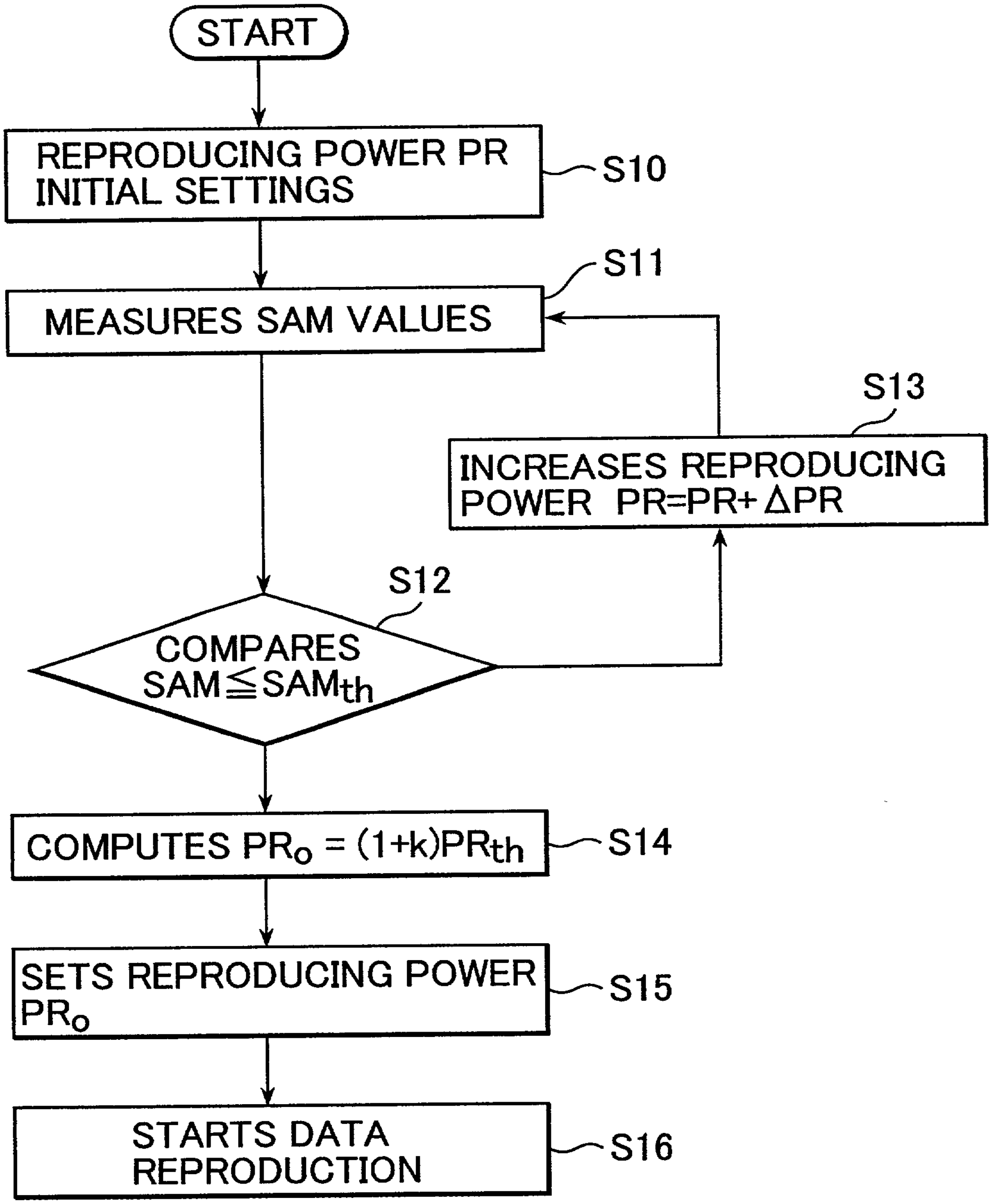

START
REPRODUCING POWER PR INITIAL SETTINGS
S10
MEASURES SAM VALUES
S11
INCREASES REPRODUCING POWER PR=PR+ΔPR
S13
COMPARES SAM≦SAMth
S12
COMPUTES PRo = (1+k)PRth
S14
SETS REPRODUCING POWER PRo
S15
STARTS DATA REPRODUCTION
S16

FIG.13

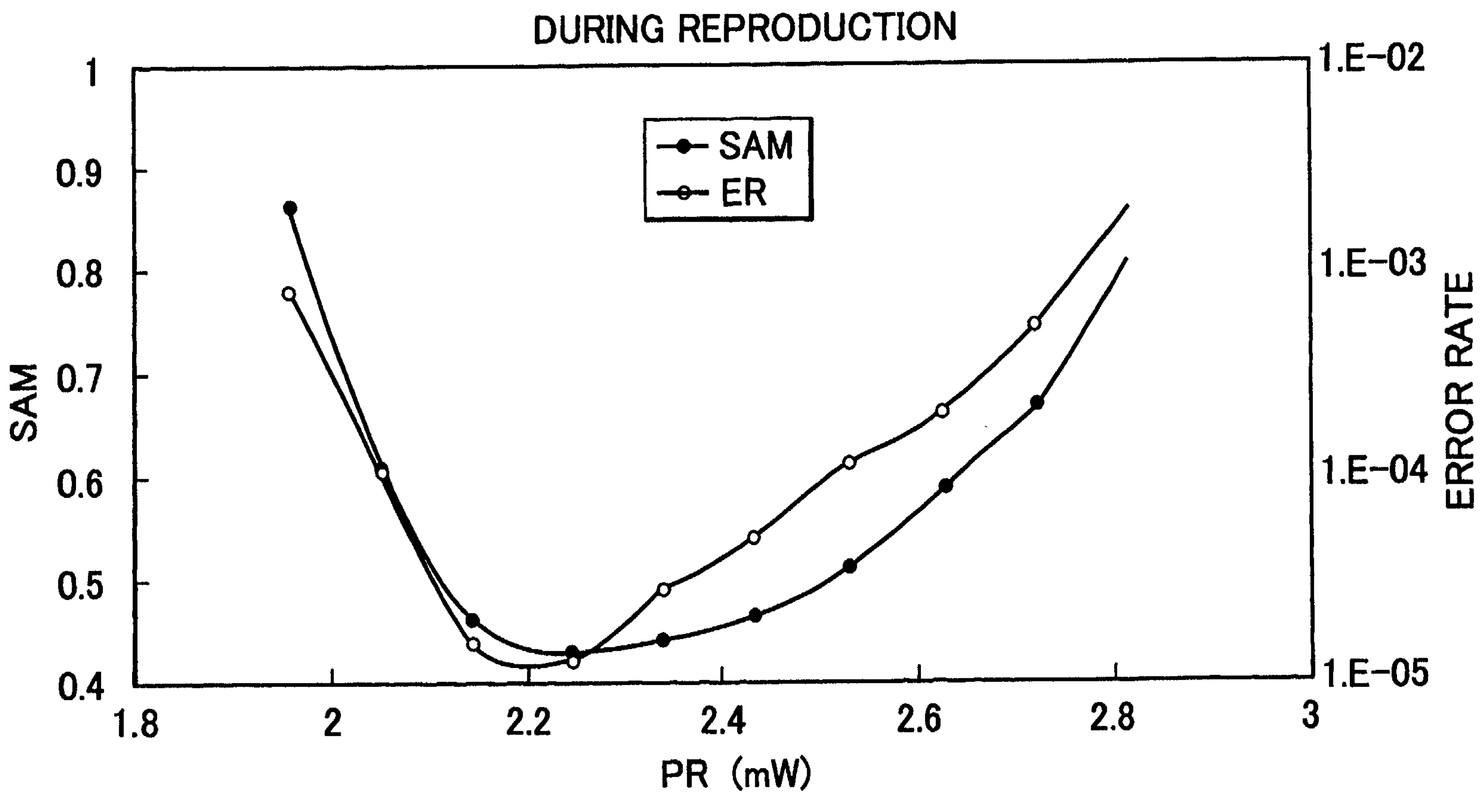

DURING REPRODUCTION
SAM
ER
SAM
ERROR RATE
1
0.9
0.8
0.7
0.6
0.5
0.4
1.E-02
1.E-03
1.E-04
1.E-05
1.8
2
2.2
2.4
2.6
2.8
3
PR (mW)

FIG.14

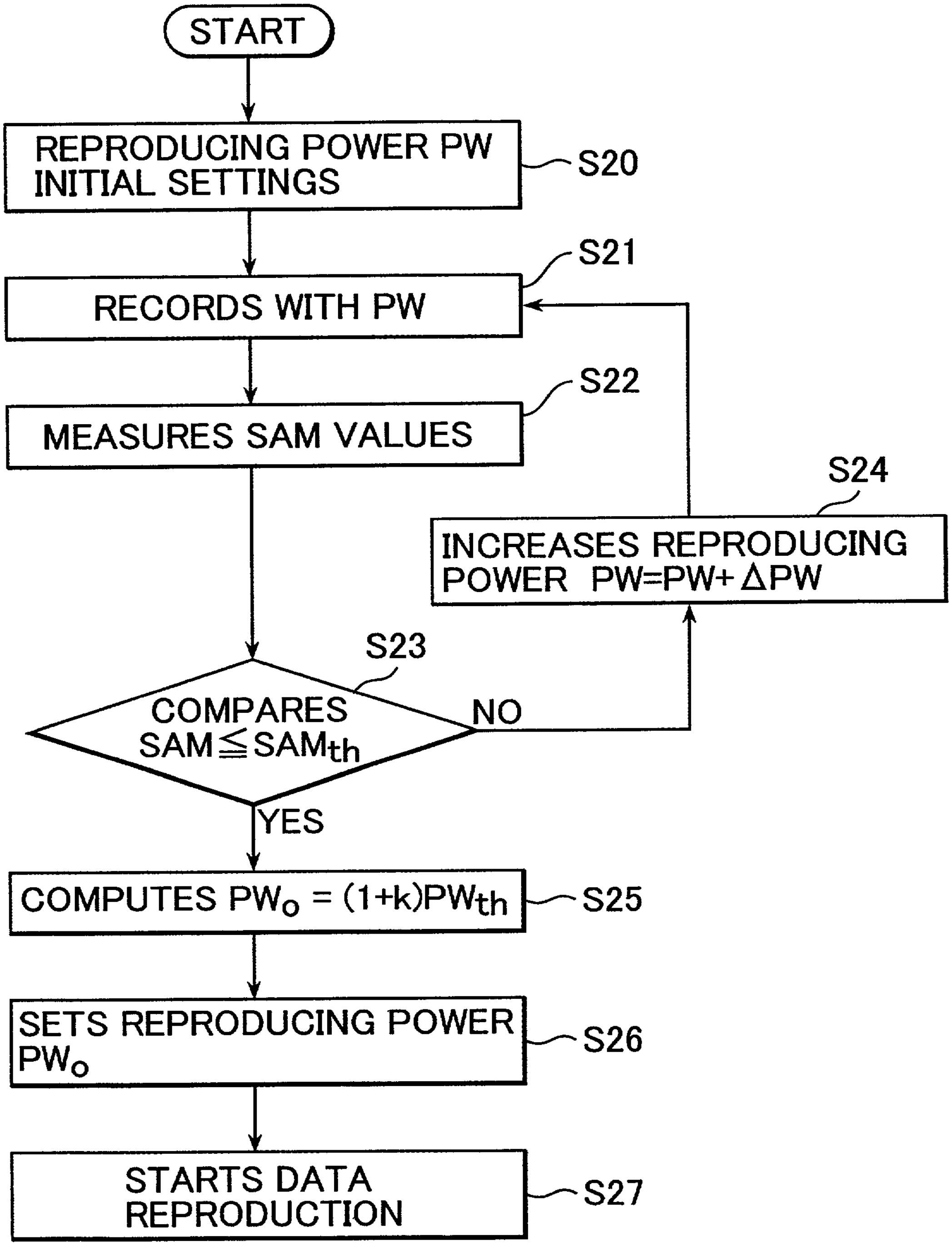

START
REPRODUCING POWER PW INITIAL SETTINGS
S20
RECORDS WITH PW
S21
MEASURES SAM VALUES
S22
S24
INCREASES REPRODUCING POWER PW=PW+ΔPW
S23
COMPARES SAM≦SAMth
NO
YES
COMPUTES PWo = (1+k)PWth
S25
SETS REPRODUCING POWER PWo
S26
STARTS DATA REPRODUCTION
S27

FIG.15

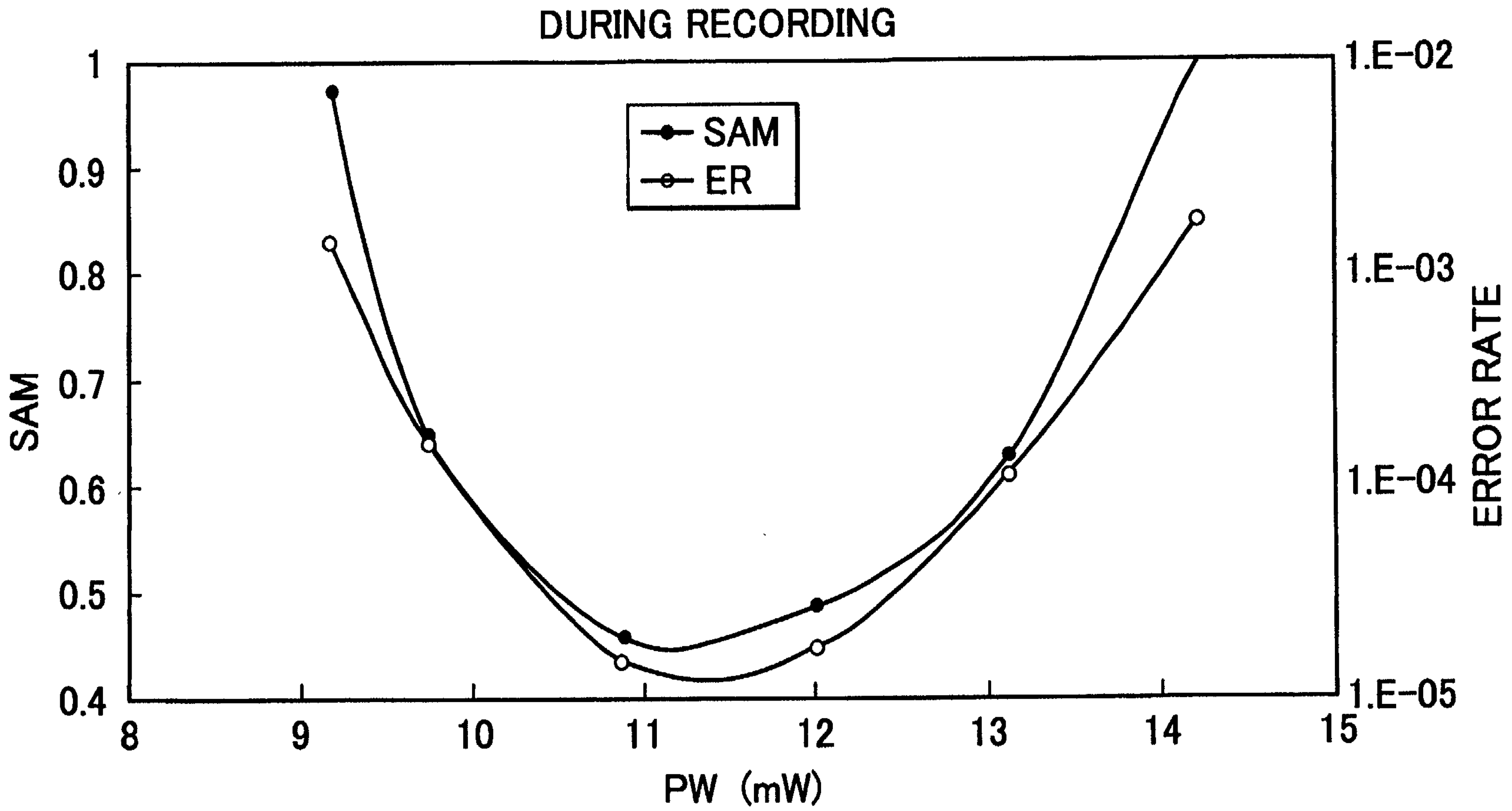

DURING RECORDING
SAM
ER
SAM
1
0.9
0.8
0.7
0.6
0.5
0.4
ERROR RATE
1.E-02
1.E-03
1.E-04
1.E-05
8
9
10
11
12
13
14
15
PW (mW)

FIG.16

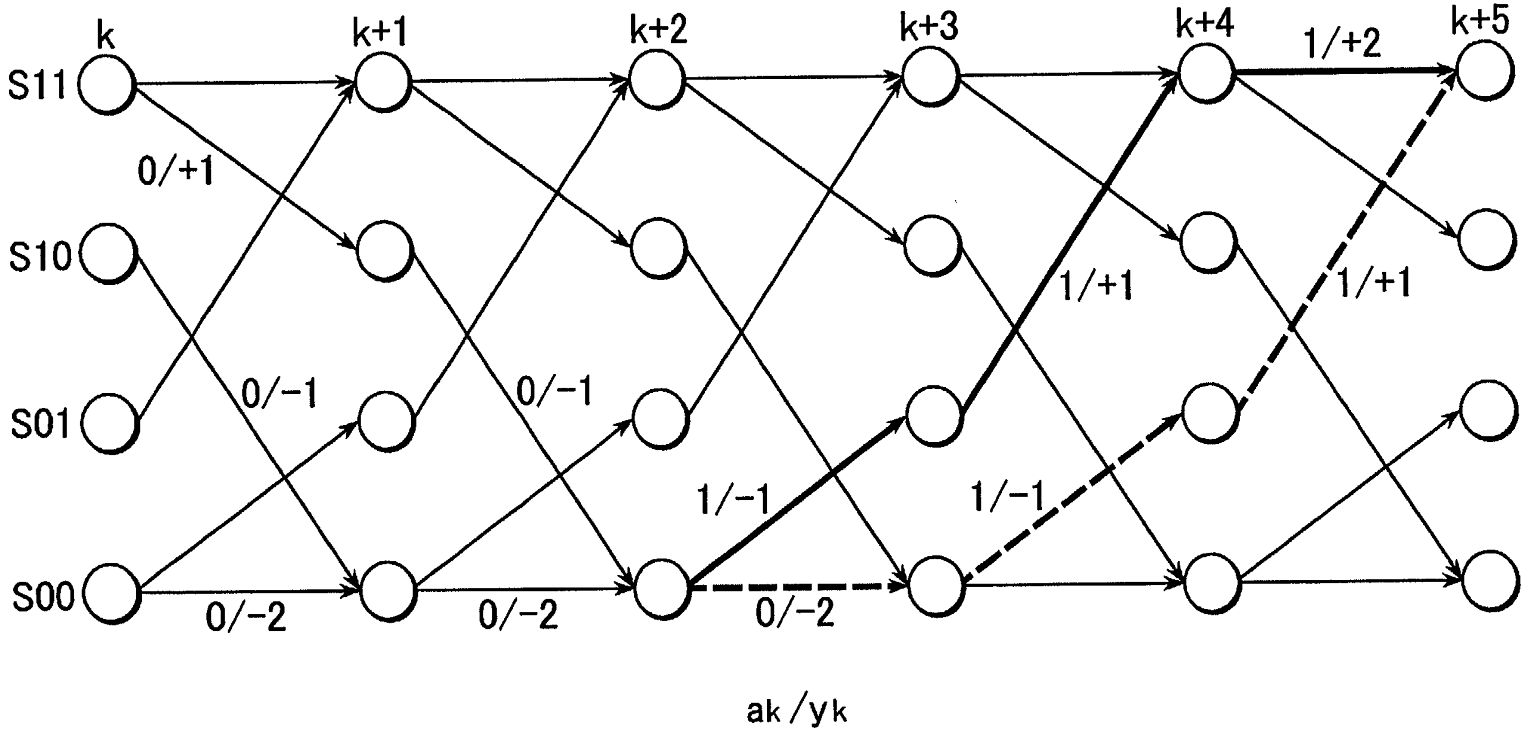

k
k+1
k+2
k+3
k+4
k+5
S11
S10
S01
S00
0/+1
0/−1
0/−2
0/−1
0/−2
1/−1
0/−2
1/+1
1/−1
1/+2
1/+1
ak /yk

FIG.17

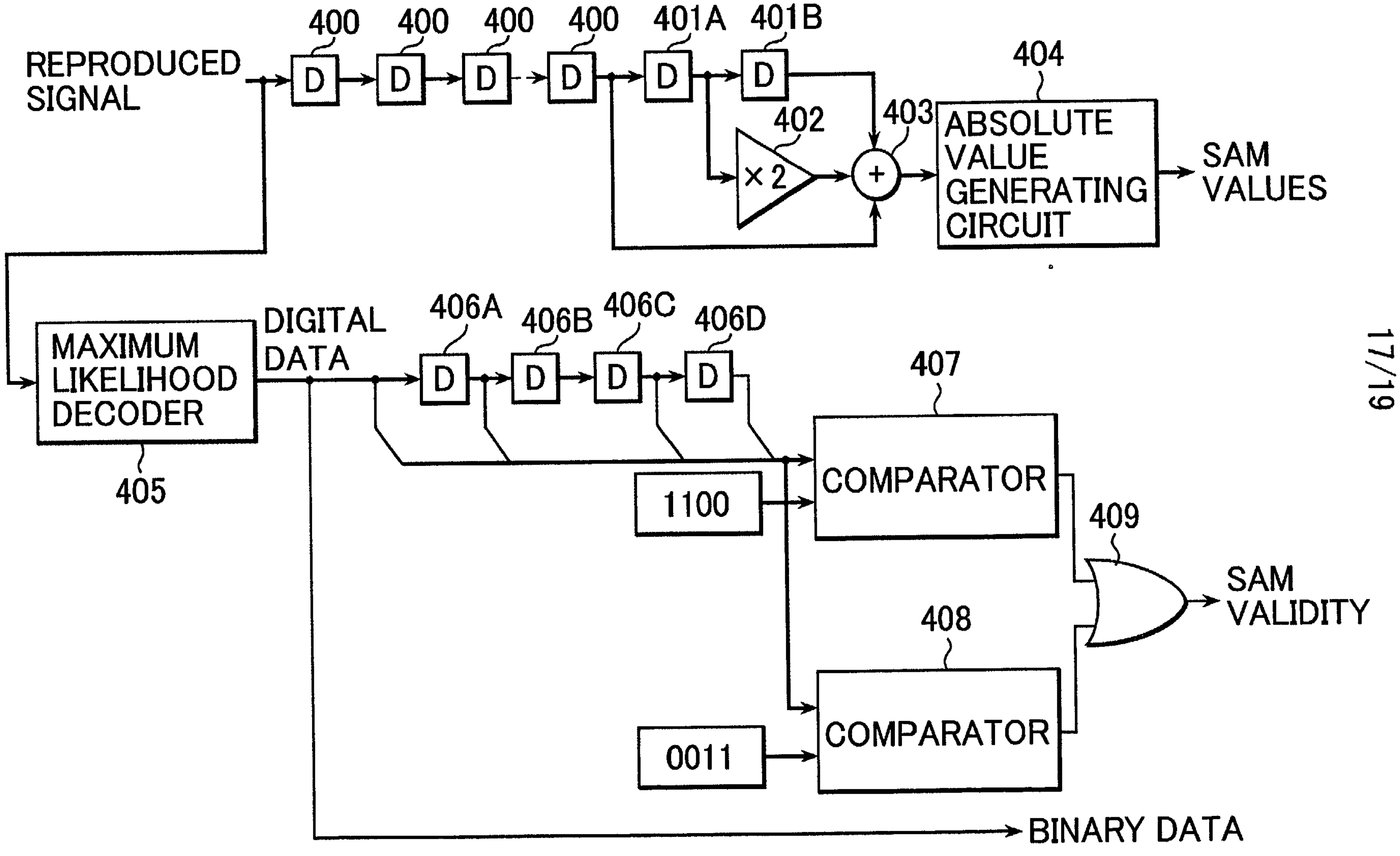

REPRODUCED SIGNAL
D
×2
+
ABSOLUTE VALUE GENERATING CIRCUIT
SAM VALUES
MAXIMUM LIKELIHOOD DECODER
DIGITAL DATA
COMPARATOR
COMPARATOR
SAM VALIDITY
BINARY DATA

FIG.18

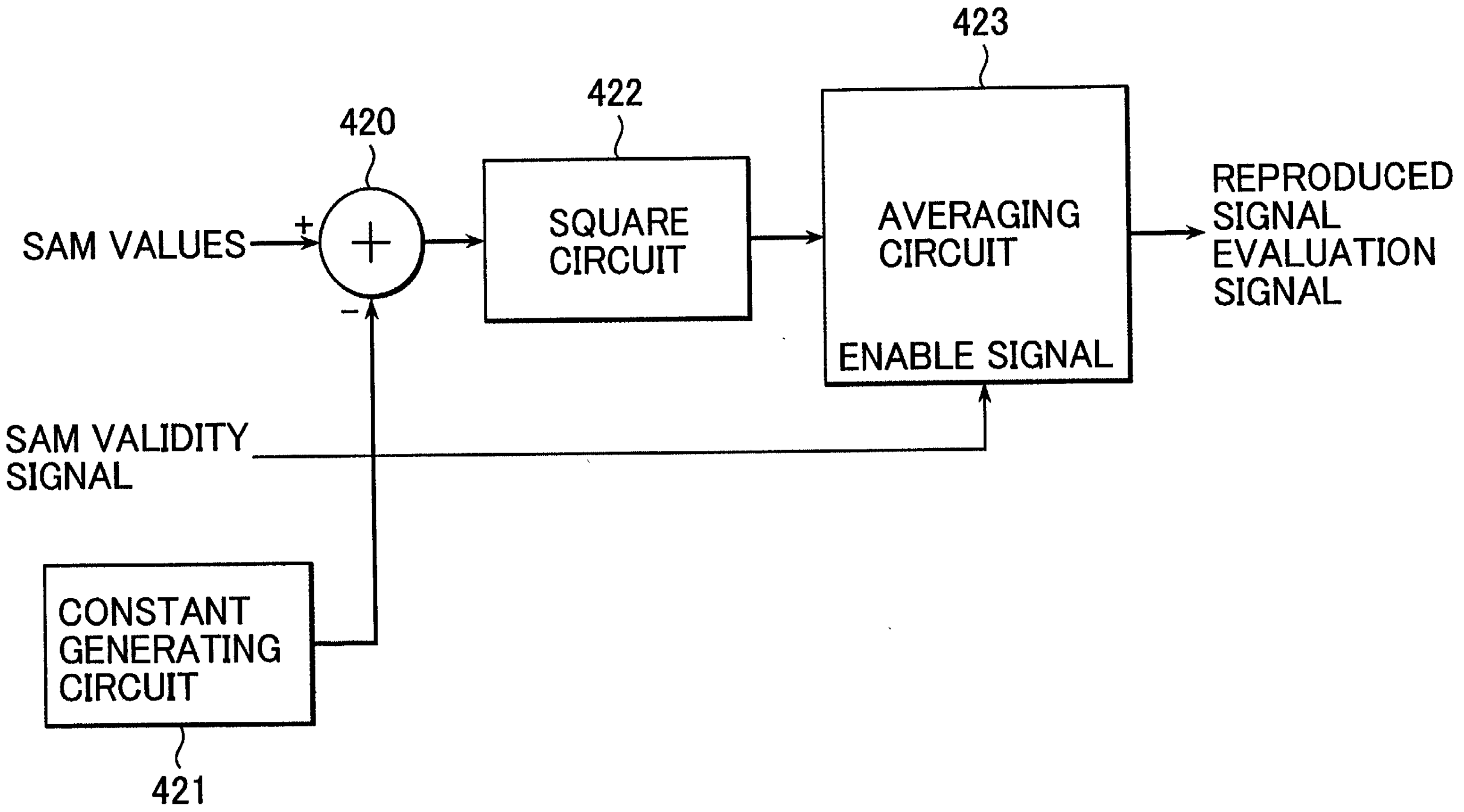
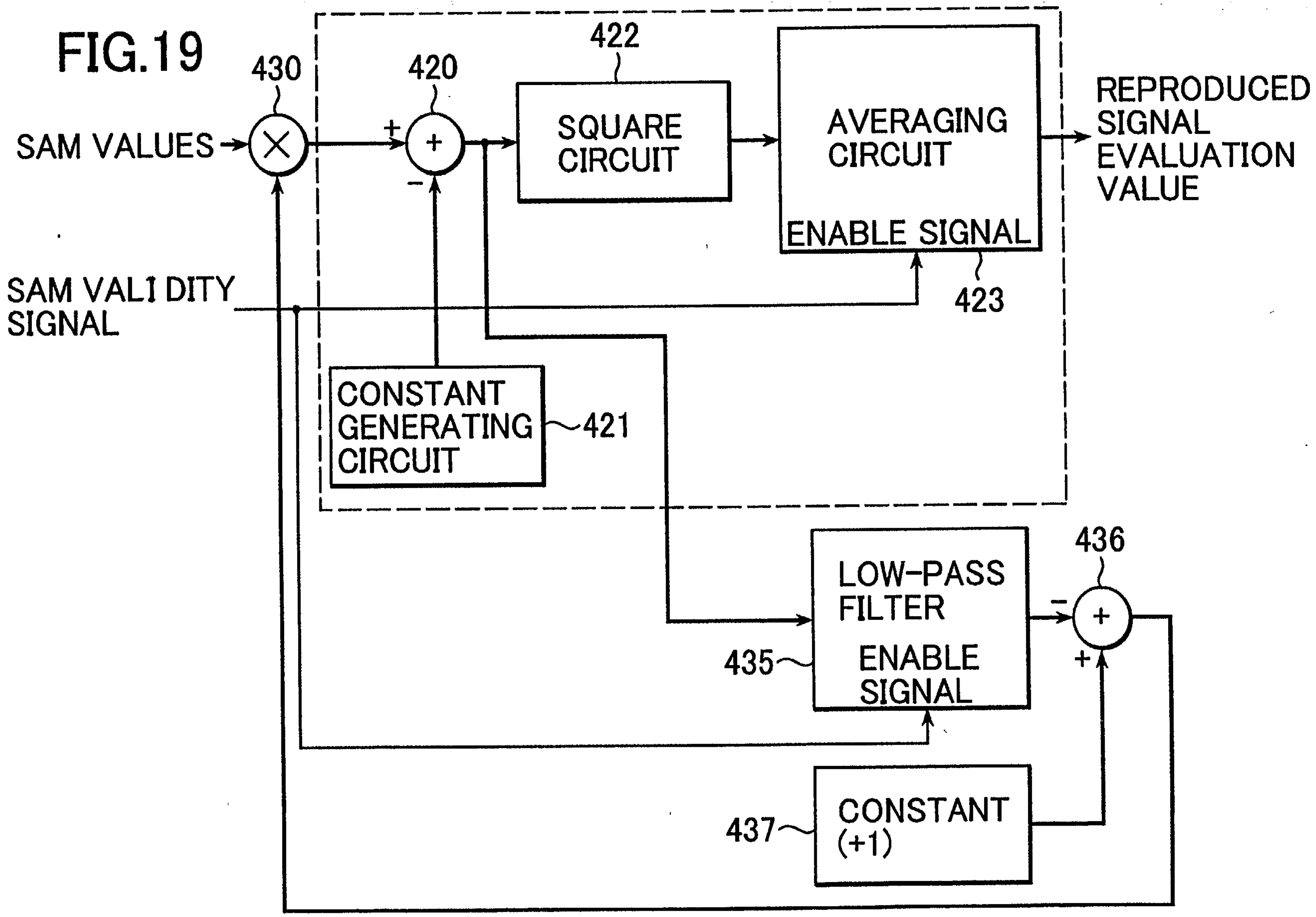

SAM VALUES
+
−
420
SQUARE CIRCUIT
422
AVERAGING CIRCUIT
ENABLE SIGNAL
423
REPRODUCED SIGNAL EVALUATION SIGNAL
SAM VALIDITY SIGNAL
CONSTANT GENERATING CIRCUIT
421

FIG.19


430
420
422
SAM VALUES
+
−
SQUARE CIRCUIT
AVERAGING CIRCUIT
ENABLE SIGNAL
REPRODUCED SIGNAL EVALUATION VALUE
SAM VALIDITY SIGNAL
423
CONSTANT GENERATING CIRCUIT
421
436
LOW-PASS FILTER
ENABLE SIGNAL
435
−
+
437
CONSTANT (+1)